REMARKS

Claims 1, 3-9, 19-22 and 25-27 remain in this application. Claim 19 has been amended. Claims 12 and 14-18 have been cancelled. Claims 1 and 19 are independent claims.

A. Claim Objections

In the Office mailed September 23, 2005, claim 12 was objected to because it contained an error. Appropriate correction was required. Claim 12 has been cancelled.

Claim 19 was also amended to correct an error. Specifically, the claim was amended to properly locate the term "switch." Rather than "an integrated circuit chip switch," the claim now correctly provides the description as a crosspoint "switch formed on an integrated circuit chip." Support for the change may be found in various portions of the application as originally filed. For example, in the second sentence of the SUMMARY OF THE INVENTION (page 2), it is stated that the equalization is typically achieved by integrating the necessary circuitry into the same integrated circuit chip as the switching matrix of the crosspoint switch.

Applicants respectfully request that the proposed amendment be entered.

B. Rejection of Claims 19-22 for Non-Enablement

Claims 19-22 were rejected under 35 U.S.C. 112, first paragraph, as allegedly failing to comply with the enablement requirement. These claims describe a method of providing equalization for a crosspoint switch formed on an integrated circuit chip. The method includes determining signal characteristics related to signal transmissions via ports of the crosspoint switch. On-chip measurements of jitter of electrical signals are provided, wherein the jitter is induced by off-chip conditions. It is alleged in the Office action that a person skilled in the relevant art would be unable to make and/or use the claimed invention because the specification allegedly does not disclose that "the jitter is induced by off-chip conditions."

As noted in MPEP 2164.04, "In order to make a rejection, the Examiner has the initial burden to establish a reasonable basis to question the

enablement provided for the claimed invention. In re Wright, 27 USPQ2d 1510, 1513 (Fed.Cir. 1993) (Examiner must provide a reasonable explanation as to why the scope of protection provided by a claim is not adequately enabled by the disclosure). Respectfully, Applicants assert that the burden has not been met by the mere statement that the specification does not disclose that the jitter is induced by off-chip conditions. Applicants secondly assert that the specification does disclose that the jitter is induced by off-chip conditions.

Applicants point out that "jitter induced by off-chip conditions" is not a method step of the claimed invention. Rather, jitter is an existing condition which is addressed by the claimed method. MPEP 2164.01 states that the test of enablement is whether one reasonably skilled in the art could make or use the invention from the disclosure coupled with information known in the art and experimentation which is not "undue experimentation." Crosspoint switches formed on an integrated chip are known. Moreover, the jitter that is induced by conditions which are "off-chip" relative to the integrated circuit chip is well known. The MPEP states, "A patent need not teach, and preferably omits, what is well known in the art." In re Buchner 18 USPQ2d 1331, 1332 (Fed. Cir. 1991). The invention described in method claim 19 is not one in which the jitter is induced, but is instead one which includes providing on-chip measurements of the jitter and at least partially basing the setting of equalization circuitry on the on-chip measurement of jitter. Since it is known that off-chip conditions will induce jitter and since a detailed description of the various off-chip conditions is not significant to the on-chip measuring, Applicants submit a person reasonably skilled in the art would be able to make and use an invention in which on-chip measurements of jitter are provided and in which equalization circuitry setting is automated and is at least partially based on the on-chip measurements of jitter. That is, the enablement requirement is satisfied.

Moreover, portions of the specification as originally filed provide disclosure that jitter is induced by off-chip conditions. In paragraph [0009] on page 3 of the specification, it is stated that for the embodiment for which the crosspoint switch is formed as a single integrated circuit chip, the chip is often connected to a printed circuit board. Thus, jitter that is generated as a result of conditions on the printed circuit board is jitter induced by off-chip conditions. Then, in paragraph [0028] on page 6 of the specification, it is stated that if the crosspoint switch is electrically connected to a printed circuit board,

each input equalization may be tailored to improve signal integrity over the circuit board trace (e.g., copper trace) of the associated input channel. Similarly, on page 12, paragraph [0044] states that for the printed circuit board 86 of Fig. 5, the transmission loss for each channel to a crosspoint switch 88 is determined, as indicated at step 100 of Fig. 6. In Fig. 5, a single copper trace 101 is included to show one connection of an input port to the first stage crosspoint switch 88. Since the distances that signals must travel from their sources to the different input ports of the different switches will vary, the skin losses for the same signal to the different input ports will differ. Variation in lengths of traces will also occur for the input channels to the first stage switch 88. As one possible measurement technique, jitter may be monitored at the output port while available levels of equalizations are tried in turn.

Applicants respectfully assert that a person reasonably skilled in the art would be able to make and use the method described in claims 19-22, since various phenomena for inducing jitter are well known in the art, since inducing jitter is not an element of the claimed invention, and since the disclosure describes the claimed method as being applied to measurements of jitter induced by off-chip conditions. Reconsideration of the rejection of claims 19-22 under Section 112, first paragraph, is requested.

C. Rejection of Claim 27 for Non-Enablement

Claim 27 was rejected under 35 U.S.C. 112, first paragraph, as allegedly failing to comply with the enablement requirement. Claim 27 is dependent upon claim 1. The dependent claim describes the equalization circuitry of claim 1 as being configured to recurringly execute jitter measurements and recurringly execute responsive selection of levels of equalization for individual input ports, thereby enabling the levels of equalization to track variations in transmission losses. It is asserted in the Office action that the specification does not disclose recurring execution of jitter measurements and recurring executions of the responsive selection of levels of equalization.

It is respectfully asserted that the specification as originally filed discloses recurring execution of measurements and recurring executions of selections of equalization. While not all of the embodiments described in the specification provide configuration as described in claim 27, the automated embodiments are described as enabling this configuration. On page 3 of the specification, paragraph [0010] describes the adaptive equalization

embodiment as one in which equalization settings are varied automatically, providing the advantage in which the level of equalization can track changes in the environment or in the supported hardware. This description is consistent with the description in claim 27. The level of equalization can track changes in the environment or in the supported hardware only if the measurements detect that a change in the environment or the supported hardware has occurred since a previous measurement. Given the description in paragraph [0010], a person reasonably skilled in the pertinent art would be enabled to make and use the invention.

Moreover, the last sentence in paragraph [0033] on page 8 of the specification states that a practical alternative to measuring transmission loss is to repeatedly adjust the equalization while monitoring the output jitter, and then select the equalization setting that provides the best results. Since the equalization is repeatedly adjusted and the output jitter is monitored as the levels of equalization are repeatedly adjusted, paragraph [0033] provides description for enabling a person skilled in the art to carry out the invention described in claim 27.

Paragraph [0049] on pages 13 and 14 of the specification compares the adaptive equalization embodiment to other embodiments of crosspoint switches described in the application. The adaptive equalization automatically adjusts the equalization setting so that it has an advantage over the adjustable equalization embodiment. Moreover, adaptive equalization tracks changes in the environment. While changes in temperature, IC processing, and supply voltages may have only a minimal effect on the optimal equalization setting, the automated adaptive equalization embodiment will allow the effect to be eliminated. While the adjustable equalization embodiment operates well within it's single setting, the adaptive equalization embodiment enables tracking of one-setting differences in equalization level without requiring the user to periodically check jitter. This is possible, since the adaptive equalization embodiment provides the periodic jitter checking described in claim 27.

It is undisputed that a person skilled in the pertinent art would be able to make and use the invention described in claim 1, which includes equalization circuitry configured to measure jitter and to automatically select levels of equalization in response to the jitter measurements. Thus, the only issue is whether such a person would be capable of enabling the jitter measurement and the equalization level selections to occur on a recurring

basis. Applicants respectfully assert that given the information provided in the pending application and the information currently known in the art, a person skilled in the art would be enabled to configure equalization circuitry to trigger recurringly as described in claim 27.

Reconsideration of claim 27 is respectfully requested.

D. The Examiner's "Response to Arguments"

Applicants note with appreciation that the Office action provides responses to the remarks submitted by Applicants in the amendment filed in September 2005. The logic provided in the portion of the Office action entitled "Response to Arguments" provides a better understanding of the basis for the rejection.

As a preliminary for the response, Applicants point out that while a number of different "approaches" to on-chip equalization for a crosspoint switch are described in the application as originally filed, the amended claims do not necessarily read on all of the different approaches. Four approaches are described in paragraph [0006] on page 2 of the application. In a first approach, a separate user-adjustable equalization circuit is provided for each input port or output port of the switch. The second approach provides adaptive equalization. Then, in the first sentence of paragraph [0010], it is stated that the adaptive equalization approach varies the equalization settings automatically so that less user intervention is required as compared to the adjustable equalization approach. The adjustable equalization approach is described in paragraph [0008] on page 2 of the application. In the adjustable equalization approach there are a number of available fixed levels of frequency-dependent equalization. On the basis of anticipated transmission loss, a target level of equalization is achieved by selectively activating and deactivating switched connections. Claim 1 describes the other approach, i.e., the adaptive equalization approach, since claim 1 states that the equalization circuitry is responsive to the jitter measurements to automatically select levels of equalization. Similarly, claim 19 states that the step of setting equalization circuitry is automated and is at least partially based on the on-chip measurements of jitter.

It is important to note that the mere teaching of equalization circuitry does not anticipate the claimed invention. Each feature of the claim must be considered. On pages 7 and 8 of the Office action mailed

September 23, 2005, the Examiner provides reasons for disagreeing with Applicants' assertions that McCormack et al. does not anticipate the method described in claim 19 and that it would not be obvious to modify McCormack et al. to include on-chip measuring of jitter and automated setting of equalization circuitry at least partially based on the on-chip jitter measurements. In support for the conclusion that McCormack et al. teaches "providing on-chip measurements of jitter of electrical signals, wherein said jitter is induced by off-chip conditions," the Examiner cites Fig. 2, block 21 of McCormack et al., as well as page 1, paragraph [0011] and page 4, paragraphs [0051] to [0056]. However, block 21 in Fig. 2 merely shows a pre-compensation network that includes capacitors and resistors. Applicants can find no support for concluding that the pre-compensation network 21 provides any measurements of jitter. Applicants request support for the assertion that the three resistors and the two capacitors of the network are capable of providing on-chip measurement of jitter.

Regarding the cited paragraph on page 1 of McCormack et al. (i.e., paragraph [0011]), this paragraph merely states that inter-symbol interference (ISI) may be mitigated in linear transmission media (not in amplifiers) by static or adaptive equalization. While this paragraph uses the term "adaptive" there is no support for concluding that the term reads on claim 19. Paragraph [0011] provides the background for the McCormack et al. invention, does not anticipate providing on-chip measurements of jitter of electrical signals, and does not anticipate providing automated settings of equalization circuitry at least partially based on on-chip measurements of jitter.

Turning now to the cited portion of page 4 of McCormack et al. (i.e., paragraphs [0051] to [0056]), there is no teaching of on-chip jitter measurements or any teaching of automated settings of equalization circuitry at least partially based on the on-chip measurements of jitter. Paragraph [0051] states that the component values of the series capacitors in block 21 of Fig. 2 are pre-selected. This leads away from Applicants' claimed invention. The pre-selection may be relevant to some approaches described in Applicants' specification, but not the claimed invention of claim 19 or claim 1. Paragraph [0052] states that the network with a modest ratio of high-to-low frequency gain allows the use of amplifiers that have half the bandwidth normally required. This is irrelevant to the determination of patentability of Applicants' claimed invention. Then, in paragraph [0053], it is stated that the

network may be applied externally to an integrated circuit. Clearly, this does not anticipate the on-chip features of the pending claims.

The Office action points out that paragraph [0054] teaches that the network includes passive elements which can be segmented and/or programmable (i.e., tunable). For instance, where the network is included in the integrated circuit, by changing upper metal layers on the integrated circuit, the elements of the network are manipulated and thus allow for easy tuning of a circuit's ISI jitter characteristics. However, programmability does not anticipate providing on-chip measurements of jitter. Nor does programmability anticipate setting equalization circuitry such that the setting is automated and is at least partially based on on-chip measurements of jitter. In the "user-adjustable equalization approach" described in Applicants' specification, there may be passive elements that are segmented and/or programmable/tunable, but this is not the approach described in independent claims 1 and 19. Paragraph [0054] provides tunability, but this is fundamentally different than providing automated setting of equalization circuitry and is unrelated to providing on-chip jitter measurements.

Paragraph [0055] describes network tuning. The network of the present invention may be implemented between each of the cascaded cross-point switch devices. This does not anticipate Applicants' claimed invention. Finally, in paragraph [0056] the connections of Fig. 2 are described. There is no reference to any capability of enabling measurements of jitter, whether on-chip or off-chip.

The burden of establishing a *prima facie* case of anticipation is satisfied only if it is shown that all of the features of a claim are described in or are inherent to a single prior art reference. Applicants respectfully assert that a *prima facie* case of anticipation has not been presented, since McCormack et al. does not teach or inherently possess on-chip jitter measurements. Moreover, the reference does not describe or inherently possess automated settings of equalization circuitry that are at least partially based on on-chip jitter measurements.

A similar approach applies to the rejection of claims 1 and 3-9, as set forth in the "Response to Arguments" section of the Office action. The previously filed remarks of Applicants with respect to the patentability of claim 1 are identified, but page 4 of the Office action asserts that the equalization circuitry of McCormack et al. is configured to measure jitter and to use the jitter measurements as a basis for offsetting transmission losses, with the

equalization circuitry being adaptive circuitry enabled to automatically select levels of equalization. Applicants respectfully assert that this position is not supported by the McCormack et al. reference. As support, the Office action cites block 201 in Fig. 1 of McCormack et al., and cites paragraphs [0008], [0037] and [0054]. Block 201 in Fig. 1 is merely described as being equalization circuitry, but there is no description of equalization circuitry being configured to measure jitter or being adaptive to automatically select levels of equalization. Paragraph [0008] merely defines the signal degradations of interest to the invention. Paragraph [0037] identifies the components of Fig. 1, including the generalized term "input signal equalization circuits." On-chip jitter measurements and automatic selections of levels of equalization are not identified. Paragraph [0054] describes programmability/tunability, but does not describe jitter measurements or automatic selections of levels of equalization.

Importantly, Applicants agree that McCormack et al. discloses an equalizer which is tunable or adjustable, as asserted by the Examiner on page 5 of the Office action. However, adjustability does not anticipate automatic selection of signal levels by equalization circuitry which is an element of a crosspoint switch integrated circuit. The Office action relies heavily upon the teaching in McCormack et al. that "by changing upper metal layers of an integrated circuit, the elements of the network are manipulated and thus allowing easy tuning of a circuit's ISI jitter characteristics" (paragraph [0054]). On the other hand, Applicants assert that this evidences that claim 1 is not anticipated by the teachings of the McCormack et al. reference. A person skilled in the art would recognize that "changing upper metal layers on an integrated circuit" is not an automatic process as described in claim 1.

The Office action also states that McCormack et al. discloses the use of active elements in Figs. 2 and 7. Applicants respectfully request that the relevance of the active elements be identified, if this is to be used as the basis for rejection. The description of Figs. 2 and 7 with regard to "active" appear to be closely tied to the capability of a user via a "programming interface." Since the programming is provided externally, it appears to lead away from Applicants' claimed invention.

Yiu was cited for its teachings regarding switchable connections that are arranged in electrical parallel, with components that include inductors and resistors. It is not asserted in the Office action that it would be obvious to modify the teachings of McCormack et al. to include on-chip jitter

measurements or to include equalization circuitry that achieves automatic selections of levels of equalization in response to the jitter measurements. Applicants assert that even if one were to modify the teachings of McCormack et al. in view of Yiu, the resulting crosspoint switch and the resulting method would not render Applicants' claimed invention unpatentable. Reconsideration of independent claims 1 and 19 and their dependent claims is respectfully requested.

E. Patentability of Claims 25 and 26

As noted in paragraph [0050] of the application as originally filed, a concern with adaptive equalization within the same IC package as the switch matrix of a crosspoint switch is that adaptive equalization of each port may require a significant portion of the total IC chip real estate. Dependent claim 25 describes a solution. The equalization circuitry of the crosspoint switch integrated circuit includes a multiplexer connected to a jitter measurement component for providing the jitter measurements. The multiplexer is connected to receive electrical signals from each of the input ports and is operatively associated with the jitter measurement component to enable the jitter measurements on a port-by-port basis. Dependent claim 26 states that the jitter measurement component includes a phase-locked loop and a voltage-controlled oscillator.

Claim 25 was rejected as allegedly being anticipated by McCormack et al. Moreover, it is stated that the use of multiplexers is admitted prior art in the specification. Regarding the admitted prior art, Applicants agree that multiplexers were known prior to the filing of the pending application. However, it is inaccurate to then conclude that every possible use of a multiplexer is "anticipated" as meant under Section 102. Under Section 102, a claimed must be considered as a whole. Under no conditions, should the specification be read to identify the combination of claims 1 and 25 to be "admitted prior art."

It is further asserted that neither Fig. 11 nor paragraphs [0080]-[0084] of McCormack et al. teaches a multiplexer operatively associated with a jitter measurement component to enable jitter measurement on a port-by-port basis. Fig. 11 in the prior art reference merely shows "active elements and a current drive source." Paragraph [0080] states that in one embodiment a drive function drives an input line to a specific state, while a sense function

senses the state of an output line. Since the input is driven to a specific state, jitter measurements cannot occur. In paragraph [0081], active elements are controlled by bits set in a programmable register. Setting appropriate bits in the programmable register turns "on" a specific active element and couples the drive line to a specific input data line. However, there is no teaching or even a suggestion that a multiplexer be operatively associated with a jitter measurement component to enable jitter measurements on a port-by-port basis.

Paragraph [0082] of McCormack et al. describes an approach for turning transistors "on." There is no description of jitter measurements. Then, in paragraph [0083] it is stated that the drive line may be used to check connection integrity of input data signals to external signal sources. Clearly, this is not a teaching regarding jitter measurements. It is also suggested that the drive line may be convenient for checking internal device operation, particularly if the drive line may be coupled to the input lines proximate the inputs of the device. This shows no teaching of incorporating a jitter measurement component into the device, as well as incorporating a multiplexer that is operatively associated with the jitter measurement component to enable jitter measurement on a port-by-port basis.

Finally, paragraph [0084] states that an output drive line may be provided for the outputs of the switch. The output drive line is multiplexed with the output signal proximate the output signal driver, with the output signal driver outputting either an output data signal or the signal on the output drive line based on contents of the switch configuration register. There is no teaching of jitter measurements.

Claim 26 was rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over McCormack et al. in view of Blazo et al. Blazo et al. was cited for its teachings regarding particular elements of a jitter measurement capability. Neither Blazo et al. nor McCormack et al. teaches or suggests providing a crosspoint switch integrated circuit having a jitter measurement component of any type. Moreover, neither reference provides the description or suggestion of the multiplexer used in the manner described in claim 25 with respect to equalization circuitry of a crosspoint switch integrated circuit. Without a reading of Applicants' disclosure, there would be no motivation in combining the teachings of the prior art in the manner described in the pending claims.

F. Patentability of Claim 27

In addition to the rejection of claim 27 under 35 U.S.C. 112, first paragraph, the Office action rejects claim 27 as being anticipated by McCormack et al. Respectfully, Applicants assert that the rejections are logically inconsistent. That is, it appears that claim 27 is being rejected because the claimed invention is fully described and known in the art and because there is not sufficient knowledge in the art to enable the invention.

Claim 27 describes recurring execution of jitter measurements by equalization circuitry of the crosspoint switch integrated circuit. In rejecting claim 27, the Office action cites block 21 in Fig. 2 of McCormack et al., as well as paragraphs [0054] to [0057]. The teachings of these portions of McCormack et al. were discussed in the enablement remarks involving claim 27. Those remarks are incorporated herein by reference. Clearly, block 21 in Fig. 2 of McCormack et al. does not show jitter measurements. The block merely shows three resistors and two capacitors. The block is a pre-compensation network. The cited paragraphs describe the network, but do not described on-chip jitter measurements and do not describe recurring executions of such measurements.

Reconsideration of claim 27 is requested.

G. McCormack et al. in View of Yiu

Since claims 15-18 have been cancelled, only claims 7 and 21 have been rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over McCormack et al. in view of Yiu. Yiu was cited for disclosing switchable connections arranged in electrical parallel and components that include inductors and resistors. Applicants assert that even if one were to modify McCormack et al. to include such switchable connections, the resulting device and method would render independent claims 1 and 19 obvious under Section 103(a).

Applicants respectfully request reconsideration of the claims in view of the amendments and remarks made herein. A notice of allowance is earnestly solicited. In the case that any issues regarding this application can

be resolved expeditiously via a telephone conversation, Applicants invite the Examiner to call Terry McHugh at (650) 969-8458.

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